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Effect of $SrTiO_3$ Deposition Temperature on the Dielectric Properties of $SrTiO_3/YBa_2Cu_3O_{7-\delta}/LaAlO_3$ Structures

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EFFECT OF $SrTiO_3$ DEPOSITION TEMPERATURE ON THE DIELECTRIC PROPERTIES OF $SrTiO_3/YBa_2Cu_3O_{7-\delta}/LaAlO_3$ STRUCTURES

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SUMMARY

We report on the effect of the deposition temperature of $SrTiO_3$ on the dielectric properties of $SrTiO_3/YBa_2Cu_3O_{7-\delta}/LaAlO_3$ thin film multilayer structures. In these structures, the $YBa_2Cu_3O_{7-\delta}$ (YBCO) films were deposited at 800°C by laser ablation, followed by the in-situ deposition of the $SrTiO_3$ (STO) layer at one of the following temperatures: 750°C, 650°C, 550°C, 450°C, 350°C, and 250°C. Gold (Au) films were deposited and patterned on top of the STO layer to form planar Au/STO/YBCO capacitor structures. The electrical response was studied by measuring the dielectric constant (ε_r) and loss tangent ($\tan\delta$) of the ferroelectric film from 300-40 K, at 1.0 MHz, and at electric fields up to 100 kV/cm. Our results show 750°C to be a deposition temperature which allows for large variations of ε_r with limited enhancement of $\tan\delta$, while lower deposition temperatures cause a reduction of the induced change in ε_r and an increase in $\tan \delta$ with applied field.

INTRODUCTION

The study of the properties of ferroelectric thin films have generated enormous interest because of their potential use in areas such as phase shifters, ferroelectric capacitors, and memory devices, amongst others[1-3]. The successful insertion of this technology in current systems demands full optimization of the material and electrical properties of the ferroelectric films. Of paramount importance is the attainability of in-plane epitaxy with the host substrate or oxide layer, since its favors the growth of a ferroelectric film with a highly textured structure. Compatibility with other materials whose properties could also result in the optimization of the working system is also critical. High Temperature Superconductors (HTS) exhibit properties that could advantageously complement those of the ferroelectric films to enhance the functionality of electronic components currently in use. The superior performance of microwave components fabricated using HTS as compared to that of their conventional conductor counterparts, has been already demonstrated[4,5]. Therefore, fabrication and characterization of HTS/ferroelectric thin film structures for the development of highly reliable, low loss, tunable microwave components, have become an area of intense research[6-8]. Because of a close lattice match (~2%)[9], as well as chemical compatibility between $SrTiO_3$ (STO) and the $YBa_2Cu_3O_{7-\delta}$ (YBCO) HTS thin films, these two materials could be favorably used to fabricate tunable microwave devices. Consequently, knowledge of the optimal deposition conditions for the growth of high quality STO films on YBCO thin films is of foremost importance. To the best of our knowledge, a detailed study of the effect of the deposition temperature of the STO film on its dielectric and structural properties as well as on the integrity of the underlying superconducting film has not been performed so far.

In this paper, we present the results of our study on the effect of the STO deposition temperature on the electrical properties of the $SrTiO_3/YBa_2Cu_3O_{7-\delta}/LaAlO_3$ (STO/YBCO/LAO) thin film multilayer structures. Our results indicate that to obtain high quality STO films which allow for a large variation of ε_r with limited enhancement in $\tan\delta$ while preserving the integrity of the underlaying superconducting film, the STO films should be deposited at temperatures near 750°C. Details on the film deposition process and multilayer structures characterization will be presented.

EXPERIMENTAL

All the STO/YBCO/LAO structures investigated in this study were fabricated in-situ by laser ablation. The structure was formed by growing the YBCO films on 4.0 mm x 10 mm x 0.50 mm (100) $LaAlO_3$ single-crystal substrates, which were held at temperatures of 800°C, followed up by the corresponding STO film. The same procedures were followed for the fabrication of all the samples except for the deposition temperature of the STO films which was different for every structure ranging from 750°C down to 250°C at intervals of 100°C. Typically, thicknesses of 350 nm and 500 nm were obtained for the YBCO films and the STO films, respectively.

The crystal structure and the surface topology of the STO films were analyzed by X-Ray Diffraction (XRD) and Atomic Force Microscopy (AFM), respectively. For the electrical characterization, thirty 400μm x 400μm x 2.5μm gold (Au) contacts were deposited by electron beam evaporation onto the STO layer. An area of approximately 1.0 mm x 4.0 mm of the STO films was chemically etched using a 7% solution of hydrofluoric acid (HF) to expose the underlying YBCO upon which a 2.5 μm Au counterelectrode was subsequently evaporated (see Figure 1). This configuration was used to measure the relative dielectric constant (ε_r) and the loss tangent ($\tan\delta$) of the STO layer as a function of an externally applied dc electric field (**E**), at 1.0 MHz, and in the temperature range from 300 to 40 K. During the measurements, the Au electrode was kept at a positive bias with respect to the YBCO electrode. The electrical measurements were performed using an HP-4192 A LF

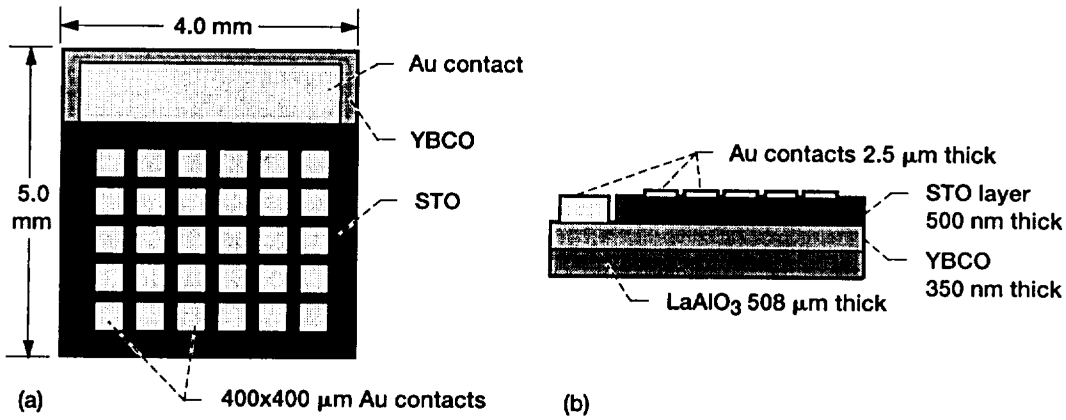

Figure 1.—Schematic representation of the configuration used to measure the electrical response of the STO layer in the STO/YBCO/LAO multilayer structure: (a) top view (b) side view.

impedance analyser and a closed-cycle helium gas refrigerator to allow for a continuous temperature sweep within the aforementioned temperature range. For the measurements, the sample was mounted on a brass sample holder which in turn was bolted to the cold finger of the refrigerator. Electrical feedthroughs at the edges of the holder allowed for electrical contact to the Au dots across the surface of the STO sample. The measurement process was fully automated and controlled by an HP 9000-300 computer. Data were taken both during the cooling and thermal cycles to account for thermal hysteresis.

To examine the integrity of the underlying YBCO thin film after the deposition of the STO film, a section of the remaining multilayer film was used to measure the transition temperature (T_c) of the YBCO film by etching part of the top STO layer as explained above. Electrical contact was achieved by hot pressing 2 mil diameter gold wire to the YBCO film. These measurements were performed using a standard four-point probe technique.

RESULTS

The values of ε_r and tanδ for the STO films, as well as their induced variation upon the application of a dc electric field, were highly dependent on the STO growth temperature. Figure 2 shows ε_r versus temperature for different electric field intensities applied across the STO film deposited at 750°C. Thermal hysteresis was not significant as evidenced by the good agreement between the data taken during the cooling and warming cycles for the field range shown in Figure 2. The ε_r of the STO film decreased by increasing the electric field, and the temperature at which the maximum ε_r was observed shifted to higher temperatures with increasing electric field. At 60 K, the change in intensity of the dc electric field decreased ε_r from 222 to 146. The tanδ corresponding to this film is shown in Figure 3. These data show that tanδ increased with respect to the zero field values by increasing the intensity of the electric field up to $8x10^4$ V/cm. However, further increases in bias caused tanδ to decrease slightly. At 60 K, tanδ ranged from 0.015 to 0.123 depending on bias. AFM images of the STO layer prior to the Au deposition (Figure 4) showed that the root mean square (rms) surface roughness of the STO film was 32 nm, and outgrowths up to 140 nm were apparent. XRD measurements show that this STO film was single phase and

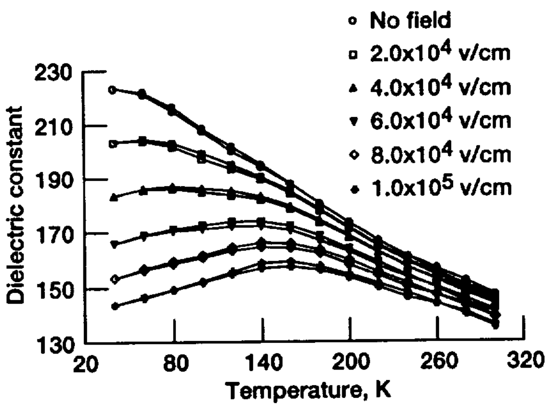

Figure 2.—Relative dielectric constant as a function of temperature and electric field for a 750 °C deposited STO layer in a STO/YBCO/LAO multilayer structure. The data were taken at 1.0 MHz.

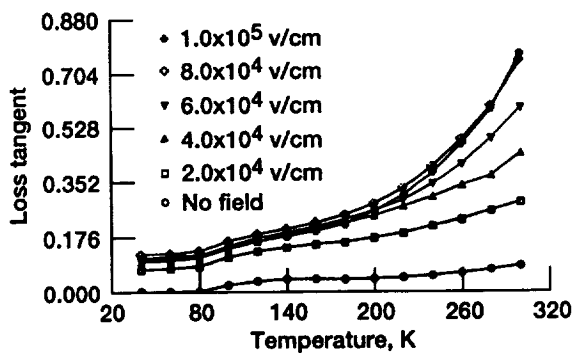

Figure 3.—Loss tangent as a function of temperature and electric field for a 750 °C deposited STO layer in a STO/YBCO/LAO multilayer structure. The data were taken at 1.0 MHz.

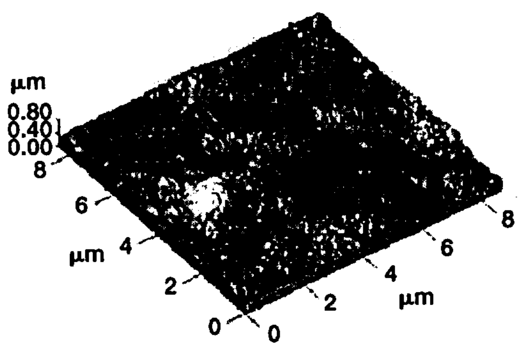

Figure 4.—Atomic Force Microscopy (AFM) micrograph showing the topology of the surface for the STO layer deposited at 750 °C.

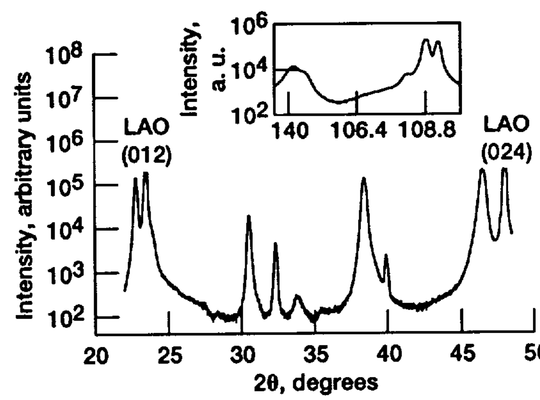

Figure 5.—2θ–ω scan for the STO layer deposited at 750 °C.

epitaxial; A 2θ-ω scan for this film is shown in Figure 5. A T_c=87.30 K was measured for the YBCO film after fabrication of the multilayer structure. Since typical T_c's for YBCO films deposited at 800°C are found to be between 88-90 K, any degradation of the YBCO due to the STO deposition was rather small.

Decreasing the STO growth temperature to 650°C, resulted in much lower ε_r values, lower tuning, and increased tanδ. Figure 6 shows that ε_r increased with decreasing temperatures, indicating that crystalline STO was formed, and was the material which dominated the electrical behavior. However, the low ε_r values indicate that the STO was poorly crystallized or that impurity phases with low ε_r were also present resulting in an overall lowering of the ε_r values. In the absence of an applied electric field, the tanδ versus temperature data exhibit values of tanδ slightly larger than those observed for the STO film deposited at 750°C. Furthermore, tanδ rises sharply when an external dc bias is applied (see Figure 7). Figure 8 shows an AFM image of the film deposited at 650°C. The surface characteristics of this film are similar to those exhibited by the film deposited at 750°C, with a rms roughness of 40 nm and outgrowths near 140 nm. A difference between the 750 and 650°C films is that the density of outgrowths is higher for the 650°C sample than for the

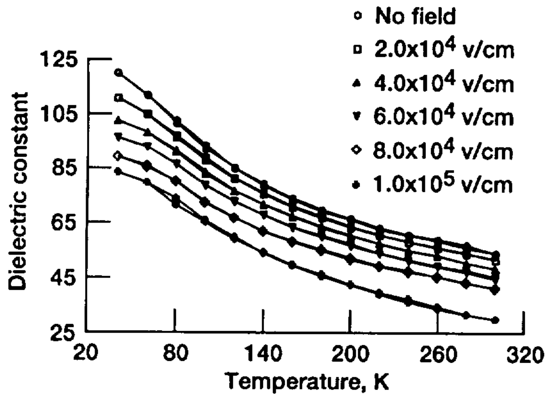

Figure 6.—Relative dielectric constant as a function of temperature and electric field for a 650 °C deposited STO layer in a STO/YBCO/LAO multilayer structure. The data were taken at 1.0 MHz.

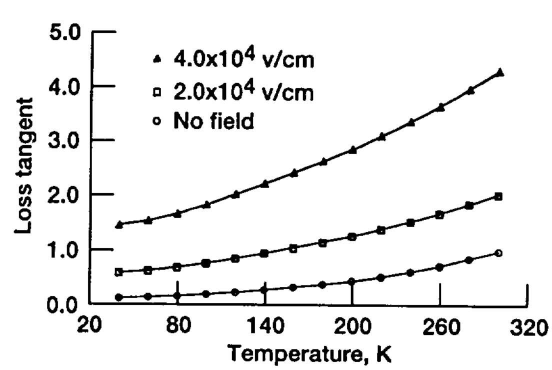

Figure 7.—Loss tangent as a function of temperature and electric field for a 650 °C deposited STO layer in a STO/YBCO/LAO multilayer structure. The data were taken at 1.0 MHz.

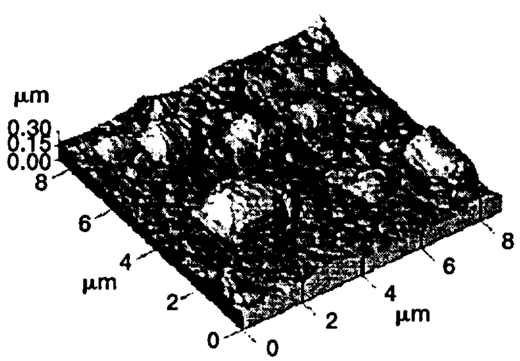

Figure 8.—Atomic Force Microscopy (AFM) micrograph showing the topology of the surface for the STO layer deposited at 650 °C.

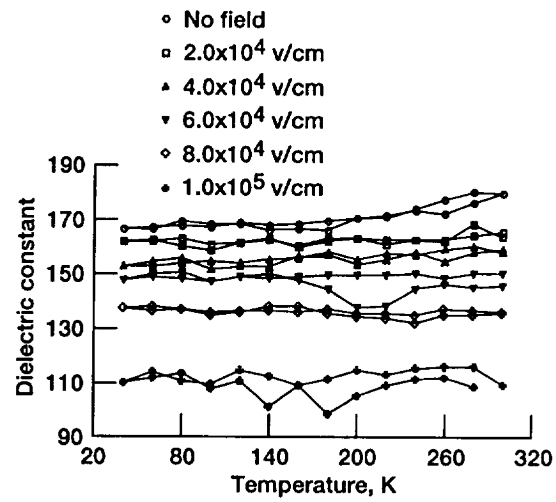

Figure 9.—Relative dielectric constant as a function of temperature and electric field for a 550 °C deposited STO layer in a STO/YBCO/LAO multilayer structure. The data were taken at 1.0 MHz.

sample deposited at 750°C. A T_c=83.79 K was measured for the YBCO film after deposition of the STO layer at 650°C.

Lowering the STO growth temperature to 550°C resulted in a film with a higher ε_r than that observed in the film deposited at 650°C, but there was no well-defined temperature dependence to the ε_r (see Figure 9). In the absence of an applied field the values of tanδ were somewhat lower than those of the film deposited at 650°C and slightly higher than those of the 750°C sample. However, similar to the 650°C sample, the tanδ for the 550°C film increased sharply under the influence of an electric field (see Figure 10). A T_c=85.82 K was measured for the YBCO film after deposition of the STO layer at 550°C.

STO films deposited at temperatures from 250-450°C showed virtually no tuning, and tanδ was high when a dc bias was applied. Figure 11 shows ε_r versus temperature data for an STO film deposited at 350°C. The ε_r values are low and drop with lower temperatures. As shown in Figure 12, increasing the bias across the films caused the tanδ to increase sharply.

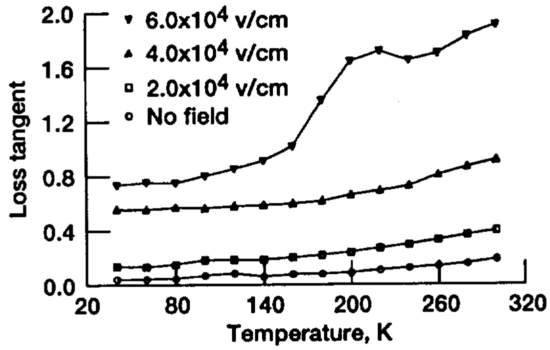

Figure 10.—Loss tangent as a function of temperature and electric field for a 550 °C deposited STO layer in a STO/YBCO/LAO multilayer structure. The data were taken at 1.0 MHz.

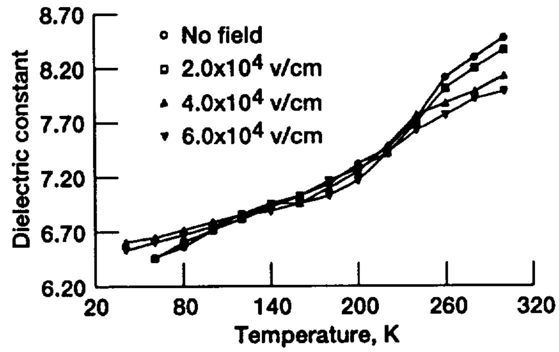

Figure 11.—Relative dielectric constant as a function of temperature and electric field for a 350 °C deposited STO layer in a STO/YBCO/LAO multilayer structure. The data were taken at 1.0 MHz.

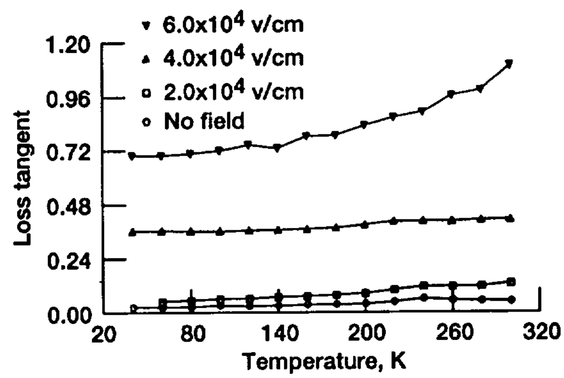

Figure 12.—Loss tangent as a function of temperature and electric field for a 350 °C deposited STO layer in a STO/YBCO/LAO multilayer structure. The data were taken at 1.0 MHz.

DISCUSSION

The only STO films in this study which displayed the electrical characteristics expected for high quality STO films were the films deposited at 750°C. The increase in ε_r with decreasing temperature and drop in ε_r when a dc bias is applied are similar to the trends observed in single crystals of STO[10], with the exception that bulk STO is an incipient ferroelectric and thus a peak in ε_r as a function of temperature is not observed[11] contrary to the behavior observed in thin films. The high tanδ observed in these films at temperatures above 90 K and the observed decrease as the temperature was lowered below the superconducting transition temperature, indicate that the tanδ at high temperatures is primarily due to resistive losses in the YBCO film, and as the temperature is lowered these losses become negligible and the losses are dominated by the STO film. At 60 K, the increase in

$\tan\delta$ for biases up to 4 volts indicates that the film is supporting electric fields up to 8×10^4 V/cm, and the small decrease in $\tan\delta$ with higher voltages indicates that the sample is nearing the onset of voltage breakdown. By contrast, interdigital capacitors comprised of highly oriented STO films and a metallization arrangement in which both terminals are located on the same surface of the film reach voltage breakdown at fields over 10^5 V/cm.[12] Thus we attribute the low breakdown voltages observed in the planar capacitors to electric field concentration at outgrowths and asperities in the STO films, which minimizes the voltage required for breakdown.

The STO film deposited at 650°C exhibited lower ε_r values, reduced tunability, and significantly higher losses with an applied field than those observed for the films deposited at 750°C. The fact that the ε_r increases with decreasing temperatures indicates the presence of the STO phase in the film, but the overall reduction of ε_r is a result of additional phases with low ε_r values. Unfortunately, quantification of the extent of STO formation using XRD is difficult because of overlapping between the STO and YBCO peaks in the XRD's 2θ-ω scan. At 60 K, $\tan\delta$ increases sharply with dc bias indicating that the breakdown voltage is lowered considerably by reducing the deposition temperature.

The ε_r values for films deposited at $T \leq 550$°C showed little temperature dependence, indicating negligible formation of the STO phase. At 60 K, the ε_r values for these films varied widely and therefore it is difficult to explain such behavior in terms of insulating dielectrics. We believe that since the breakdown voltages were readily exceeded in these films, the ε_r behavior was primarily controlled by free carrier transport and charge trapping at the electrode/STO interface or at defect sites such as grain boundaries in the STO films.

AFM data show similar surface roughness and grain size for films deposited at 550-750°C. Therefore, the difference in electrical behavior can not be attributed to the charge transport along microscopic defects such as debris from the target. Films deposited at 750°C have less outgrowths and exhibit highly faceted grains, indicating textured growth of the STO films. For films deposited at 650°C and 550°C the grains are more rounded, indicating less texture, and also exhibit a higher density of outgrowths than their 750°C counterpart. AFM images of films deposited at $T \leq 450$°C were blurred because particles on the surface of the films dislodged when the AFM needle was scanned across the film. This indicates that the films were granular and did not adhere well to the substrate.

CONCLUSIONS

Deposition of $SrTiO_3$ thin films with high ε_r values, large tunability, and high breakdown voltages requires the film to be deposited at elevated temperatures. At 60 K, the ε_r of film deposited at 750°C decreased by 35 percent when an electric field of 1×10^5 V/cm was applied. The $\tan\delta$ of the film deposited at 750°C increased slightly with dc bias, and increased sharply with dc bias for all films deposited at $T \leq 650$°C. STO films deposited at 650°C exhibited reduced ε_r values and tunabilities, but the increase in ε_r with decreasing temperature suggest that there was some formation of STO. We conclude that for tuning applications, the growth temperature of STO films deposited on YBCO must be near 750°C so as to insure high voltage breakdown strengths in the films.

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13. ABSTRACT ***(Maximum 200 words)***

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